

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,976	05/02/2001	Jason Seung-Min Kim	2100653-991390	7302
26379	7590	05/11/2004	EXAMINER	
GRAY CARY WARE & FREIDENRICH LLP 2000 UNIVERSITY AVENUE E. PALO ALTO, CA 94303-2248			BANANKHAH, MAJID A	
			ART UNIT	PAPER NUMBER
			2127	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/847,976

Applicant(s)

KIM, JASON SEUNG-MIN

Examiner

Majid A Banankhah

Art Unit

2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application filed on May 02, 2001. Claims 1-20 are considered for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokic al. (U.S.Pat. No. 6,145,007, hereinafter Dokic).

Per claims 1, and 17, a system for facilitating inter-processor communication in a multiple processor computer

system having one or more shared resources (col. 1, lines 35-39, and col. 4, lines 48-62, interprocessor communication), comprising:

a first register associated with a first processor for indicating the status of the shared resources in the system and for sharing one or more tasks among the multiple processors (col. 2, lines 19-29, first register and first processor);

a second register associated with a second processor for indicating the status of the shared resources in the system and for sharing one or more tasks among the multiple processors (col. 2, lines 19-29, second register and second processor processor),

and a semaphore unit for indicating the status of the shared resources in the system and for

Art Unit: 2127

notifying the first and second processors of a particular task to be executed by the respective processors (col. 9, line 49 to col. 10 line 6, and lines 35 to col. 11 line 15, semaphore register and message communication and different states).

While the reference of Dokic teaches of communication mailbox (col. 9, lines 49-54, and see Fig 2, I/O BUS A , and I/O BUS B, Fig. 3, IPC Registers 1302), he fails to teach of two mailboxes, one associated with the first processor and the other associated with the second processor for status indication and interprocessor communication. However, it would have been obvious for one ordinary skill in the art at the time the invention was made to use one mailbox associated with the first processor DSPA and one associated with the second processor and allow the semaphore register to coordinate interprocessor communication between the mailboxes instead of registers, for the reason that both processors can read and write at the same time for the reason to be able to avoid conflict between accessing at the same time.

Per claim 2, the system of Claim 1, wherein the first processor is a host processor and the second processor is a co-processor. In the system of Dokic, Since the two processor working cooperatively, one is host and the other (DSP B) is a co processor.

Per claim 3, the system of Claim 1, wherein the tasks are shared among the multiple processors without latency. This limitation is statement of intended result, however, the system of Dokic also ensure minimum latency (col. 15, 43-55, ensure minimum latency).

Art Unit: 2127

Per claim 4, the system of Claim 1, wherein either the first or second mailbox receives a message from the semaphore unit indicating a task to be executed, and wherein the first or second mailbox notifies its associated processor of the message. The system of Dokic teaches of the limitation in col. 15, lines 43-55, and col. 16, lines 15-19.

Per claim 5, the system of Claim 4, wherein either the first or second mailbox causes a respective interrupt signal to be communicated to its associated processor when a message is received from the semaphore unit. Dokic teaches of the semaphore and interrupt logic in col. 10, lines 7-34.

Per claim 6, the system of Claim 5, wherein, in response to the respective interrupt signal, the associated processor services the interrupt signal by reading the message from the associated mailbox. Dokic teaches of interrupt signal and read/write messages from the mailbox in col. 10, lines 35-61.

Per claim 7, the system of Claim 6, wherein upon reading the message from the associated mailbox, the mailbox is cleared and an acknowledge notification is communicated by the mailbox to the other processor to indicate that the mailbox is empty and that the task is being executed. Dokic teaches of the limitation in (setting the flag and clearing the flag) in col. 10, lines 35-61.

Per claim 8, the system of Claim 1, wherein the semaphore unit comprises a first plurality of semaphore registers for indicating the status of a shared resource in the system and a second

Art Unit: 2127

plurality of semaphore registers for indicating messages that are communicated to the first and second mailboxes to notify a respective processor of a task to be executed. The reference of Dokic teaches of semaphore registers in col. 10, lines 62 to col. 11, line15.

Per claim 9, the system of Claim 8, wherein the semaphore registers are controlled by a semaphore controller. The semaphore register in Dokic synchronizes communication and therefore it is a semaphore controller (See col. 10, lines 35-40).

Per claim 10, the system of Claim 8, wherein the first plurality of semaphore registers comprises a first register for indicating the status of a shared resource in the systems a second register for setting particular bits in the first register to indicate the data stored in a particular memory location of the shared resource, and a third register for clearing particular bits in the first register. Dokic teaches of setting bits in the register to indicate the status of the memory in col. 10, lines 35 to col. 11, line 15.

11. The system of Claim 10, wherein the first, second, and third registers are 32 bit registers.

Per claim 12, the system of Claim 10, wherein the first register comprises a first bit portion wherein each individual bit is associated with a particular shared resource in the system, and a second bit portion for indicating the data stored in a particular memory location of that particular shared. Setting the bits in a registry is programmer's choice and does not constitute a patentable

Art Unit: 2127

limitation. However, Dokic teaches of setting the bits in the registry in col. 12, line 59 to col. 13, line 14.

Per claim 13, the system of Claim 12, wherein the first bit portion comprises six bits such that the most significant bit in the first bit portion is associated with a host instruction memory, the next most significant bit in the first bit portion is associated with a ping buffer, the next most significant bit in the first bit portion is associated with a pong buffer, the next most significant bit in the first bit portion is associated with a coprocessor instruction memory, the next most significant bit in the first bit portion is associated with a cache memory, and the least significant bit in the first bit portion is associated with input/output resources. The reference of Dokic teaches of ping-pong strategy in col. 12, lines 37-48.

Per claim 14, the system of Claim 12, wherein in response to being notified of a task to be executed, the respective processor reads the data from the first register to execute the task. Dokic teaches of semaphore register and read in col. 10, line 35 to col. 11, line 15.

Per claim 15, the system of Claim 8, wherein the second plurality of registers comprises a fourth register and a fifth register each for indicating a message for the respective mailboxes of a task to be executed. Register mailbox is taught by Dokic in col. 10, lines 35-61.

16. A system for facilitating inter-processor communication in a multiple processor computer system having one or more shared resources (U.S. Pat., No. 6,009,389), comprising:

Art Unit: 2127

means for cooperatively multitasking and interruptively multitasking among the multiple processors (col. 8, lines 39-46, pre-planned interruption of the current task),

means for notifying a respective processor of a particular task to be executed (col. 7, lines 24-37, message sent from the external PC to the processor),

means for indicating the status of the shared resources in the system (col. 2, lines 19-29, second register and second processor), and

means for communicating the status of a particular shared resource to the processor for execution of the task (col. 9, line 49 to col. 10 line 6, and lines 35 to col. 11 line 15, semaphore register and message communication and different states).

While the reference of Dokic teaches of pre-planned interruption the tasks, he fails to teach of preemption. However, preemptive multitasking or time slice multitasking by definition is a form of multitasking in which the operating system periodically interrupt the execution of a program and passes control of the system to another waiting program. In the system of Dokic, planned interruption can be interpreted as periodic interruption, as sending a periodic interruption is a form of pre-planning, for the reason to give all the task a chance to be executed and no task be starved for processing time. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to make the O.S. send periodic interruption in order to interrupt the execution of the program and pass control to the waiting program preemptively, so that no takes all the processing time.

Art Unit: 2127

Per claim 18, the method of Claim 17, wherein the notifying step comprises the step of interrupting the first processor with an interrupt signal. Dokic teaches of a interrupt-based communication in col. 5, lines 29-37, and col. 7, lines 9-23.

Per claim 19, see the rejection of claim 7.

Per claim 20, see the rejection of claim 8.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

**Commissioner of Patent and Trademarks
Washington, D.C. 20231**

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington, VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Majid Banankhah

4/30/04

MAJID BANANKHAH
PRIMARY EXAMINER